IN THE CLAIMS:

1. (previously presented) A processing system for accessing memory, comprising:

an address bus for providing a first address and a second address to memory, wherein the first address follows the second address on the address bus without any intervening addresses on the address bus;

a data bus for receiving information from memory; and

first means for generating a first sequence signal that when negated indicates that the first address may not be sequential to the second address, a second sequence signal that when negated indicates that the first address is not sequential to the second address, and a third sequence signal that when negated indicates that the first address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the first address, if it is an instruction address, is sequential to the immediately preceding instruction address.

2. (previously presented) The processing unit of claim 1, wherein if the first address is not sequential to the second address, the first sequence signal is negated prior to the second sequence signal being negated.

3. (previously presented) A processing system for accessing memory, comprising;

an address bus for providing a first address and a second address to memory, wherein the first address follows the second address on the address bus without any intervening addresses on the address bus;

a data bus for receiving information from memory;

an execution unit which generates branch conditions and data addresses;

a decode control unit which decodes instructions; and

a fetch unit, coupled to the execution unit, the decode control unit, the address bus, and the data bus, for generating a first sequence signal that when negated indicates that the first address may not be sequential to the second address, a second sequence signal that when negated indicates that the first address is not sequential to the second address, and a third sequence signal that when negated indicates that the first address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the first address, if it is an instruction address, is sequential to the immediately preceding instruction address.

4. (Original) The processing system of claim 3, wherein the decode control unit comprises an instruction register.

5. (previously presented) The processing system of claim 3, wherein the fetch unit comprises:

an address control unit, coupled to the decode control unit and the execution unit, for receiving a branch condition signal from the execution unit and a branch decode signal and a load/store signal from the decode control unit and for providing the first, second, and third sequence signals.

6. (Original) The processing system of claim 5, wherein the execution unit comprises a condition generator that provides the branch condition signal.

7. (Original) The processing system of claim 6, wherein the execution unit comprises a data address generator which provides a data address signal to the fetch unit.

8. (previously presented) The processing system of claim 7, wherein if the first address is not sequential to the second address, the first sequence signal is negated prior to the second sequence signal being negated.

9. (previously presented) The processing system of claim 3, wherein if the first address is not sequential to the second address, the first sequence signal is negated prior to the second sequence signal being negated.

10. (currently amended) A processing system for fetching instructions and data, comprising;

an address bus for providing a current address for retrieving a first instruction, the first instruction stored at the current address in an instruction memory, a previous address for retrieving a second instruction, the second instruction stored at the previous address in the instruction memory, and a data address for retrieving data, wherein the data address occurs before the current address and after the previous address, and wherein the current address follows the previous address without any intervening addresses for retrieving instructions;

a data bus for retrieving the first and second instructions and the data; and

a fetch unit, coupled to the address bus and the data bus, for generating a first sequence signal that when asserted for the current address indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address, wherein the asserted or negated first sequence signal is provided with the current address for use by the instruction memory, and wherein when the address bus provides an address for retrieving data that is not an instruction, the first sequence signal is negated.

11. (Original) The processing system of claim 10, wherein the fetch unit comprises:

an address control unit for receiving a branch condition, a branch decode signal, and a load/store signal and for providing the first sequence signal.

12. (previously presented) The processing system of claim 11, further comprising:
an execution unit which provides the branch condition; and
a decode control unit which provides the branch decode signal and the load/store signal.

13. (previously presented) A processing system comprising:
an execution unit;
a decode control unit;
a fetch unit, coupled to the execution unit and the decode control unit, for providing addresses on an address bus which may be sequential, and providing a first sequence signal and a second sequence signal for each address provided on the address bus wherein the first sequence signal indicates whether each address provided on the address bus may be sequential to an immediately preceding address on the bus and the second sequence signal indicates whether each address provided on the bus is sequential to the immediately preceding address on the bus, and wherein if the second sequence signal corresponding to one of the addresses indicates that the address is not sequential to the immediately preceding address,
the first sequence signal corresponding to the address indicates that the address may not be sequential to the immediately preceding address prior to the second sequence signal indicating that the address is not sequential to the immediately preceding address, and
the second sequence signal indicates that the address is not sequential to the immediately preceding address in response to resolving a conditional branch.

14. (cancel)

15. (previously presented) The processing system of claim 13, wherein the addresses may be instruction addresses, and wherein the fetch unit further provides a third sequential signal which indicates whether each address that is an instruction address is sequential to a previous instruction address.

16. (Original) The processing unit of claim 15, wherein the execution unit comprises a condition generator that provides a branch condition signal to the fetch unit.

17. (Original) The processing unit of claim 16, wherein the decode control unit provides a branch decode signal and a load/store signal to the fetch unit.

18. – 20. (cancel)

21. (previously presented) The processing unit of claim 2, wherein the second sequence signal is negated in response to resolving a conditional branch.

22. (cancel)

23. (previously presented) The processing unit of claim 2, wherein if the first address is not sequential to the second address, the first and second sequence signals are negated during a same clock cycle.

24. (previously presented) A processing system for accessing memory, comprising;

an address bus for providing a first address and a second address to memory, wherein the first address follows the second address on the address bus without any intervening addresses on the address bus;

a data bus for receiving information from memory;

an execution unit which generates branch conditions and data addresses;

a decode control unit which decodes instructions; and

a fetch unit, coupled to the execution unit, the decode control unit, the address bus, and the data bus, for generating a first sequence signal that when negated indicates that the first address may not be sequential to the second address, a second sequence signal that when negated indicates that the first address is not sequential to the second address, and a third sequence signal that when negated indicates that the first address, if it is an instruction address, is not sequential to a previous address that was an

instruction address, wherein if the first address is not sequential to the second address, the first sequence signal is negated prior to the second sequence signal being negated and the first and second sequence signals are negated in a same clock cycle during which the first address is provided.

25. (previously presented) The processing system of claim 13, wherein if the second sequence signal indicates that an address is not sequential to the immediately preceding address, the first signal indicates that the address may not be sequential to the immediately preceding address in a same clock cycle as the second sequence signal indicating that the address is not sequential to the immediately preceding address.

26. (previously presented) The processing unit of claim 21, wherein if the first address is not sequential to the second address, the first and second sequence signals are negated during a same clock cycle.

27. (cancel)